Characteristics of Silicon Carbide Nanowires Synthesized on Porous Body by Carbothermal Reduction

Jung-Hun Kim and Sung-Churl Choi*

Division of Materials Science and Engineering, Hanyang University, Seoul 04763, Korea

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ABSTRACT

We synthesized silicon carbide (β -SiC) nanowires with nano-scale diameter (30 - 400 nm) and micro-scale length (50 - 200 μ m) on a porous body using low-grade silica and carbon black powder by carbothermal reduction at 1300 - 1600°C. The SiC nanowires were formed by vapor-liquid-solid deposition with self-evaporated Fe catalysts in low-grade silica. We investigated the characteristics of the SiC nanowires, which were grown on a porous body with Ar flowing in a vacuum furnace. Their structural, optical, and electrical properties were analyzed with X-ray diffraction (XRD), transmission electron microscopy (TEM), and selective area electron diffraction (SAED). We obtained high-quality SiC single crystalline nanowire without stacking faults that may have uses in industrial applications.

Key words : SiC, One-dimensional nanostructure, Porous body, Stacking fault

1. Introduction

In the recent past, one-dimensional (1D) nanostructures with nanometer diameters, such as nanowires, nanorods, and nanotubes, have attracted increased interest due to their optical, electrical, and mechanical properties. Potential applications range from probe microscopy tips to interconnections in nanodevices. Therefore, current researchers have focused on developing industrial methods and improving available applications for large-scale synthesis of high-quality crystalline nanostructures.¹⁻³⁾ Silicon carbide (SiC) is an important wide band gap semiconductor with superior properties, such as high breakdown field strength, high thermal conductivity, high saturation drift velocity, and excellent physical and chemical stability.⁴⁾ The use of modern SiC technologies has led to a rapid improvement in the material quality of SiC and has made practical SiC devices a reality. Researchers from different fields have proposed several approaches, such as carbon-nanotube confined reaction, chemical vapor deposition, laser ablation, arc discharge, sol-gel methods, and carbothermal reduction for growth of 1D SiC nanostructures using bottom-up processes.⁵⁻⁹⁾ There exist multiple methods for growing 1D SiC whiskers and wires, but controlling stacking faults and other defects during synthesis still remains a challenge. Stacking faults are usually found in 3C-SiC structures and affect their various properties.¹⁰⁾ Seo *et al.* preformed studies on various morphologies and stacking fault insertions in SiC whiskers grown using carbothermal reduction.¹¹⁾ They

successfully controlled the morphologies and fault angle in SiC whiskers for use as a reinforcement in composite materials. In this study, we synthesized β -SiC nanowires with diameters in nanoscale range on a porous body and silicon wafer substrate using low-grade silica and carbon black powder via carbothermal reduction at 1400°C. We then investigated their structural characteristics.

2. Experimental Procedure

In carrying out the carbothermal reduction process for growth of SiC nanowires, we used a vacuum furnace (10^{-2} - 10^{-3} Torr, 2400°C maximum temperature) with inert Ar gas. Lower grade silica (purity: 97.5%, Samchun Pure Chemical Co., Korea) and amorphous carbon black powder (Purified Carbon Black, < 200 nm, SUPELCO, USA) were chosen as the starting materials as they have the advantage of inducing high reactivity. The starting materials were fabricated using the porous bar-type ($5 \times 1 \times 0.5$ cm³) green body mixed with silica and carbon black powder with 1 : 3 wt% ratio. The porous green body enabled material sources to be evaporated for growth of SiC nanowires in the carbothermal reduction process. An Si substrate (wafer with (100) exposed plane) was located close to the porous body in order to compare the nanowires grown on the porous body (β -SiC) and those grown on the Si wafer (SiC). SiC nanowires were grown at 1300 - 1600°C temperature, 30 - 180 min holding time, and Ar gas flow rate in the 500 - 2,000 sccm range. However, we chose SiC nanowire samples that were grown at temperatures below 1450°C because the Si substrate melted at higher temperatures. Ar gas was introduced to maintain an inert atmosphere during the heat-up period. After the furnace was cooled to room

*Corresponding author : Sung-Churl Choi

E-mail : choi0505@hanyang.ac.kr

Tel : +82-2-2220-0505 Fax : +82-2-2291-6767

temperature, a gray layer on the porous body surface and light green layer on the Si wafer surface were observed.

The morphologies of PBSiC and SWSiC nanowires were observed and analyzed using scanning electron microscopy (SEM; Tescan Vega TS 5136XM, Czech Republic). X-ray diffraction (XRD; Rigaku-GDX-XRD, Rigaku Co., Japan) was used to determine the crystalline phases and measure and compare the stacking fault content in the nanowires.¹⁰⁾ Stacking faults in individual nanowires were characterized using high-resolution transmission electron microscopy (HRTEM; Tecnai G2 F30 S-Twin, FEI, USA)) images and selective area electron diffraction (SAED) patterns. Energy dispersive spectra (EDS) were obtained using an HRTEM equipped with an energy-dispersive spectroscopy (EDS) system.

3. Results and Discussion

In order to grow 1D SiC nanowires by carbothermal reduction, we started with a porous body composed of silica and carbon black powder. The overall reaction in the porous body between each of the powders for producing SiC is as follows:

In fact, Eq. (1) proceeds through two stages in which silicon monoxide (SiO) gas is formed as a vapor phase intermediate. The first step consists of a solid-solid or solid-liquid type of reaction between carbon and silica, leading to the formation of silicon monoxide and carbon monoxide (CO) vapor phases according to Eq. (2). Eq. (3) shows the second step, where silicon monoxide subsequently reacts with carbon to form SiC. Silicon monoxide obtained from Eq. (2) reacts with carbon to yield SiC nuclei heterogeneously on the surface of carbon, which is the commonly accepted mechanism of bulk SiC formation.¹²⁾ However, the vapor-liquid-solid (VLS) growth mechanism is well-known. Silicon-carrying and carbon-carrying liquid droplets are formed by melting metallic catalysts that were added intentionally. The evaporated silicon and carbon atoms diffuse across the droplet and deposit to form SiC nanowires.¹³⁾

Figure 1 shows a schematic diagram for the growth of PBSiC nanowires by vapor phase reaction through pore channels. During the growth of the PBSiC nanowires, silica and carbon black powder reacted with the evaporating silicon monoxide and carbon monoxide vapor inside the powder surface. At that time, Fe metal catalysts, which were induced by impurities in low-grade silica, diffused out of the surface of the silica particles and formed droplets. Finally, SiC nanowires were synthesized on the surface of the porous body with Fe catalysts acting as nucleation sites.

Figure 2 shows the microstructures of PBSiC (Fig. 2(a), (c)) and SWSiC nanowires (Fig. 2(b), (d)) obtained using

Fig. 1. Schematic diagram for the growth of SiC nanowires on a porous body by vapor phase reaction through pore channels.

scanning electron microscopy. All of the as-grown SiC nanowires were prepared at 1400°C temperature for a duration of 1 h. The PBSiC nanowires grown on the surface of the porous body exhibited a wide variation in diameter within the 30 - 400 nm range and a length of over 50 μm. Fig. 2(c) clearly shows a liquid droplet at the end of the nanowire, which typically occurs during VLS growth.¹⁴⁾ The SWSiC nanowires grown on silicon wafer ((100) growth plane) were observed to have a relatively uniform diameter of less than 50 nm. The diameter difference in PBSiC nanowires may be due to the silicon monoxide generation rate that depends on the pore size of the porous body. In general, the diameter of the SiC whiskers decreases with increasing silicon monoxide generation rate¹³⁾ implying that this generation rate is an important process factor in device fabrication. In other applications, it allows for nanowire handling and enables growth of structures with high surface area.

Figure 3 shows low-magnification TEM images and the corresponding EDS spectra (inset images) of the SiC nanowires for impurity analysis. Fig. 3(a) shows the metal tip in the end of the nanowire, which was determined to be Fe. The presence of about 4.25 wt% of various metal impurities such as Fe, Mg, Na, Ca, and K was shown from a formal chemical analysis of silica. Among the impurities, Fe played the role of catalyst in during VLS growth. Fig. 3(b) indicates that inner or outer in the nanowires was not detected other impurity as well as amorphous and oxide layer. Despite the high reaction temperature, the absence of oxides is due to the reduction reaction caused by carbon contained in the raw material.

Fig. 2. Microstructures of as-grown PBSiC ((a), (c)) and SWSiC nanowires ((b), (d)) (grown at 1400°C for 1 h). Images were captured using scanning electron microscopy.

Fig. 3. A low-magnification TEM image and the corresponding EDS spectra (inset images) of SiC nanowires for impurity analysis.

Figure 4 shows the X-ray diffraction patterns of the PBSiC and SWSiC nanowires prepared by the carbothermal reduction process. All the samples could be indexed to a zincblende structure β -SiC (3C-SiC). Fig. 4(a) also shows the

presence of another body, which was determined to be silica in a transformed crystalline phase (cristobalite) in the porous body at high temperature. The intensity ratio of the XRD peak at 33.6 and 41.4° $I_{33.6}^{\circ}/I_{41.4}^{\circ}$ in the PBSiC and

Fig. 4. X-ray diffraction pattern of the (a) PBSiC and (b) SWSiC nanowires prepared by carbothermal reduction. All the samples could be indexed to a zincblende structure β -SiC (3C-SiC).

SWSiC nanowires was 0.83 and 1.80, respectively. The intensity ratio increased with increasing stacking fault content.^{15,16} XRD results confirmed that the stacking fault density of SWSiC was greater than that of PBSiC nanowires.

The HRTEM and SAED (inset in figures) analyses of the PBSiC (Fig. 5(a)) and SWSiC (Fig. 5(b)) nanowires are shown Fig. 5. The SAED patterns of all samples recorded along the [110] zone axis show that the nanowires have cubic zincblende structure with growth along the [111] direction. The bright field image and its analysis establish that the PBSiC nanowire has a smooth surface with 120 nm diameter. No evident stacking faults or twin defects were found in the HRTEM image. No streak was observed in the SAED pattern (see the inset image in Fig. 5(a)) for this sample, which demonstrated that this nanowire has a nearly perfect single crystalline structure. In contrast to the PBSiC nanowire, the SWSiC nanowire was found to have a rough surface and more stacking faults. The SAED pattern of the SWSiC nanowire shows some featureless streaks and spots, which imply that SWSiC has a disorderly layered structure perpendicular to its growth direction.¹¹⁾

The above results imply that an SWSiC nanowire plays an important role in the formation of stacking faults. It could be explained that the number of stacking faults is related to the nanowire diameter, i.e., the number of stacking faults increases with decreasing nanowire diameter.¹⁷⁾ According to the axial next-nearest neighbor Ising (ANNNI) model,¹⁸⁾ SiC whiskers with stacking faults have a lower energy than those without stacking faults. Furthermore, the formation of stacking faults promotes [111] facets, which have much lower surface free energy than in other directions, such as [211] or [110]. Therefore, with regards to energetic considerations, the formation of stacking faults

Fig. 5. HRTEM and SAED (inset in figures) images of the (a) PBSiC and (b) SWSiC nanowires.

during SWSiC nanowire growth is favorable due to the contribution of the stacking faults themselves and the [111] facets at the lateral surface. The specific lateral surface area of the nanowires becomes relatively large when the nanowire diameter is small. This may enhance the formation of stacking faults to reduce the contribution of lateral surface energy.

In addition, the free-standing SWSiC nanowires on silicon substrate allow the effect of stress generated due to the lattice mismatch with the substrate to be excluded. Induced stress acts as a driving force for defect generation. The exclusion of stress effects should contribute to the fabrication of single crystalline SiC nanowires with defects. The result indicates that more stacking faults can also be formed in the SWSiC when the diameter is small and stress is generated by lattice mismatch between the nanowires and the substrate.

4. Conclusions

We report a large-scale synthesis method for SiC nanowires using a porous body and silicon substrate for industrial applications, along with their structural characteristics. SiC nanowires were fabricated from a low-grade silica and carbon black powder using simple carbothermal reduction at high temperature (1300 - 1600°C). PBSiC nanowires with various diameters (30 - 400 nm), long lengths (50 - 200 μm), and high aspect ratios were formed by reaction of silicon monoxide and carbon monoxide through the porous body pore channels. SWSiC nanowires with narrow diameters and more structural defects were synthesized on a silicon substrate at a location near the porous body. All samples were identified as single crystalline β -SiC with growth along the [111] direction. The growth mechanism was discussed in terms of VLS. Chemical analysis of metal tip at the end of the nanowire, as seen in the EDS image, confirmed the role of Fe as a growth catalyst. Fe was induced by impurities in the low-grade silica powder. XRD and HRTEM results confirmed that the SWSiC nanowires contained more defects due to their smaller diameters compared to PBSiC nanowires, which results in a lattice mismatch with the substrate. If the pore size distribution of the porous body can be controlled, it will be possible to synthesize defect-free SiC nanowires with uniform diameter for industrial applications, such as nanowire-enhanced structural ceramics and nanowire-based devices.

REFERENCES

1. P. Alivisatos, "Semiconductor Clusters, Nanocrystals, and Quantum Dots," *Science*, **271** [5251] 933-37 (1996).
2. E. W. Wong, P. E. Sheehan, and C. M. Lieber, "Nanobeam Mechanics: Elasticity, Strength, and Toughness of Nanorods and Nanotubes," *Science*, **277** [5334] 1971-75 (1995).
3. H. Dai, E. W. Wong, Y. Z. Liu, S. S. Fan, and C. M. Lieber, "Synthesis and Characterization of Carbide Nanorods," *Nature*, **375** 769-72 (1995).
4. Z. Wang, S. Wang, C. Zhang, and J. Li, "First Principles Study of the Electronic Properties of Twinned SiC Nanowires," *J. Nanopart. Res.*, **13** [1] 185-91 (2011).
5. X. T. Zhou, N. Wang, H. L. Lai, H. Y. Peng, I. Bello, N. B. Wong, C. S. Lee, and S. T. Lee, " β -SiC Nanorods Synthesized by Hot Filament Chemical Vapor Deposition," *Appl. Phys. Lett.*, **74** [26] 3942 (1999).
6. Y. B. Li, S. S. Xie, X. P. Zou, D. S. Tang, Z. Q. Liu, W. Y. Zhou, and G. Wang, "Large-Scale Synthesis of β -SiC Nanorods in the Arc-Discharge," *J. Cryst. Growth*, **223** [1-2] 125-28 (2001).
7. W. S. Shi, Y. F. Zheng, H. Y. Peng, N. Wang, C. S. Less, and S. T. Lee, "Laser Ablation Synthesis and Optical Characterization of Silicon Carbide Nanowires," *J. Am. Ceram. Soc.*, **83** [12] 3228-30 (2000).
8. C. H. Liang, G. W. Meng, L. D. Zhang, Y. C. Wu, and Z. Cui, "Large-Scale Synthesis of β -SiC Nanowires by Using Mesoporous Silica Embedded with Fe Nanoparticles," *Chem. Phys. Lett.*, **329** [3-4] 323-28 (2000).
9. G. Q. Jin, P. Liang, and X. Y. Guo, "Novel Method for Synthesis of Silicon Carbide Nanowires," *J. Mater. Sci. Lett.*, **22** [10] 767-70 (2003).
10. M. E. Brito, Y. Bando, M. Mitomo, and S. Saito, "Microstructural Features of Sintered $\text{Si}_3\text{N}_4/\text{SiC}$ -Whisker Composites: Mechanical Integrity of Whiskers," *J. Mater. Sci.*, **29** [1] 250-54 (1994).
11. W. S. Seo, K. Koumoto, and S. Aria, "Morphology and Stacking Faults of β -Silicon Carbide Whisker Synthesized by Carbothermal Reduction," *J. Am. Ceram. Soc.*, **83** [10] 2584-92 (2000).
12. J. Qian, J. Wang, and Z. Jin, "Preparation of Biomorphic SiC Ceramic by Carbothermal Reduction of Oak Wood Charcoal," *Mater. Sci. Eng., A*, **371** [1-2] 229-35 (2004).
13. J. V. Milevski, F. D. Gac, J. Petrovic, and S. R. Skaggs, "Growth of Beta-Silicon Carbide Whiskers by the VLS Process," *J. Mater. Sci.*, **20** [4] 1160-66 (1985).
14. R. D. Jong, R. A. McCauley, and P. Tambuyser, "Growth of Twinned β -Silicon Carbide Whiskers by the Vapor-Liquid-Solid Process," *J. Am. Ceram. Soc.*, **70** [11] C388-41 (1987).
15. W. S. Seo and K. Koumoto, "Stacking Faults in β -SiC Formed during Carbothermal Reduction of SiO_2 ," *J. Am. Ceram. Soc.*, **79** [7] 1777-82 (1996).
16. H.-J. Choi and J. G. Lee, "Stacking Faults in Silicon Carbide Whiskers," *Ceram. Int.*, **26** [1] 7-12 (2000).
17. L. Wang, H. Wanda, and L. F. Allard, "Synthesis and Characterization of SiC Whiskers," *J. Mater. Res.*, **7** [1] 148-63 (1992).
18. C. Cheng, R. J. Needs, and V. Heine, "Inter-Layer Interactions and the Origin of SiC Polytypes," *J. Phys. C: Solid State Phys.*, **21** [6] 1049 (1988).